

REMARKS/ARGUMENTS

Claims 1-25 are pending. Claims 1, 6-8, 11-12, 16 and 19 have been amended. In view of the following, all of the claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, then the Examiner is requested to schedule a teleconference with the Applicants' attorney to further the prosecution of the application.

Objection to claims 1-3 and 5-17 under 35 U.S.C. §112, second paragraph

Claims 6-7, 11 and 16 have been amended to correct informalities.

Rejection of claims 1 and 8-9 under 35 U.S.C. §102(a) as being anticipated by AAPA

Claim 1

Claim 1, as amended, recites an integrated circuit comprising a plurality of pins and at least one respective scan path per pin.

For example, referring, e.g., to FIG. 5 and paragraph 20 of the present application, an I/O pin 31 is coupled to a respective scan path 36. It should be noted that I/O pin 31 is both an input and an output pin, and I/O pin 31 is the only pin connected to scan path 36.

The Applicants' admitted prior art (AAPA), on the other hand, does not disclose an integrated circuit comprising a plurality of pins and at least one respective scan path per pin. Instead, AAPA discloses a scan path 9 coupled to both an input pin 2 and an output pin 12 (FIG. 1). Because the input pin 2 and the output pin 12 both share the same scan path 9, each pin does not have its own respective scan path. Therefore, AAPA does not satisfy the limitations of claim 1.

Claim 8

Claim 8, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claim 9

Claim 9 is patentable by virtue of its dependency from independent claim 8.

Rejection of claims 2-7 and 10-25 under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Chennupati (US 6,833,728)

Claim 12

Claim 12, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 1. Furthermore, Chennupati does not teach a respective scan path per I/O pin. Instead, Chennupati simply teaches a bidirectional pin 152 used to couple a device 150 to another device 102 through a transmission line 180 (Figure 1). However, this has nothing to do with testing a device for errors, let alone testing a device having a respective scan line per I/O pin. In fact, after reviewing Chennupati in its entirety, the Applicants' attorney is unable to find any mention of DUTs or scan lines whatsoever. As a result, not only is there no motivation to combine AAPA with Chennupati, but Chennupati does not even teach the limitations of claim 12 missing from AAPA. Therefore, modifying the teachings of AAPA by incorporating the teachings of Chennupati would not satisfy the limitations of claim 12.

Claim 19

Claim 19, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 12.

Claims 2-7, 10-11, 13-18 and 20-25

Claims 2-7, 10-11, 13-18 and 20-25 are patentable by virtue of their respective dependencies from independent claims 1, 8, 12 and 19.

CONCLUSION

In light of the foregoing remarks, claims 1-25 are now in condition for allowance, which is respectfully requested.

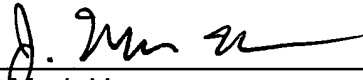
Applicants do not believe that any fees are due as a result of this filing. However, in the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner contact the Applicants' attorney at (425) 455-5575.

DATED this 18th day of September, 2006.

Respectfully submitted,

GRAYBEAL JACKSON HALEY, LLP



J. Mark Han
Registration No. 57,898
Attorney for Applicants
155 - 108th Avenue N.E. Suite 350
Bellevue, WA 98004-5973
(425) 455-5575
Fax: (425) 455-1046